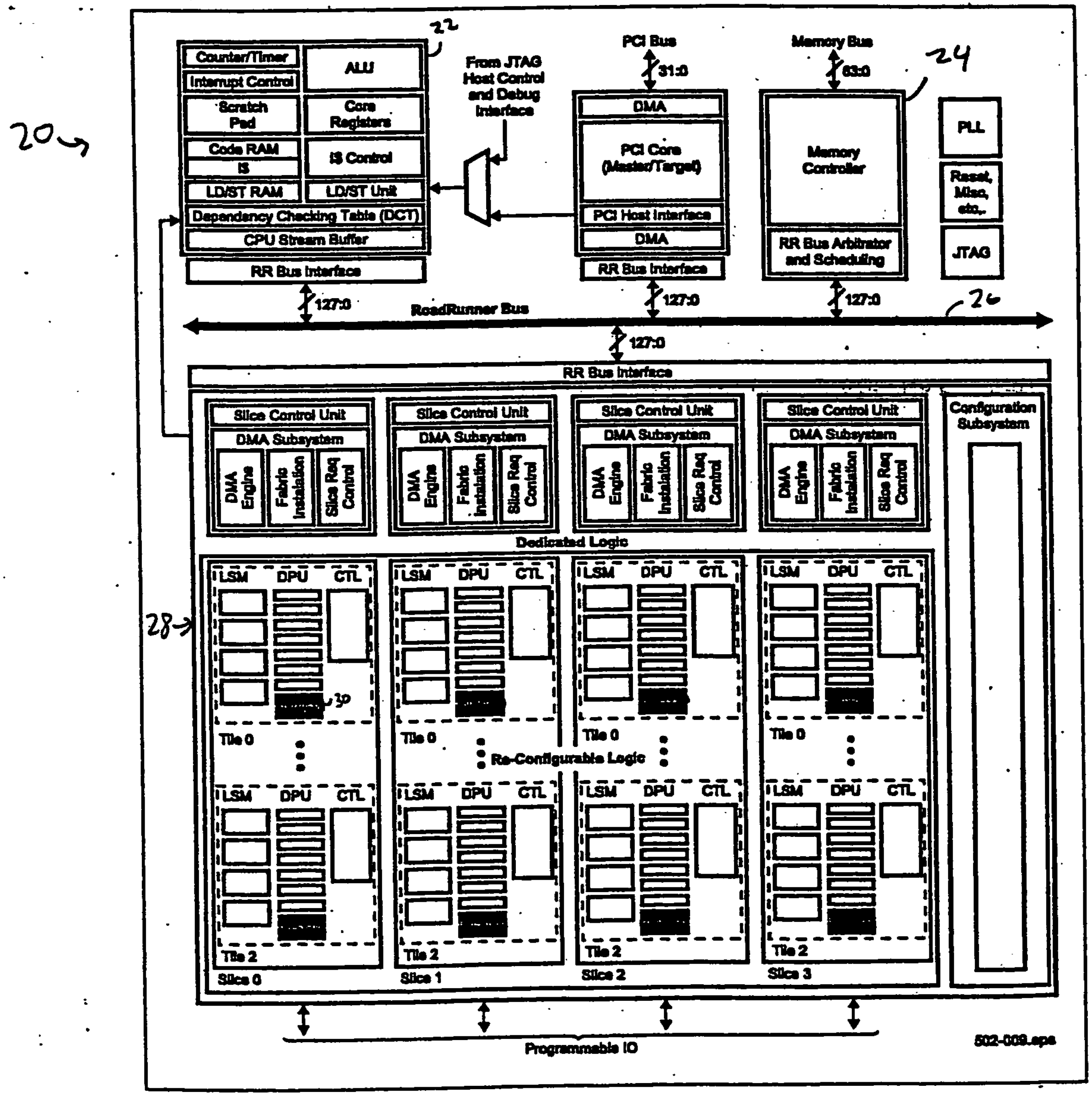

20
22
Counter/Timer
Interrupt Control
ALU
Scratch Pad
Core Registers
Code RAM
IS
IS Control
LD/ST RAM
LD/ST Unit
Dependency Checking Table (DCT)
CPU Stream Buffer
RR Bus Interface
From JTAG Host Control and Debug Interface
PCI Bus
31:0
DMA
PCI Core (Master/Target)
PCI Host Interface
DMA
RR Bus Interface
Memory Bus
63:0
24
Memory Controller
RR Bus Arbitrator and Scheduling
PLL
Reset, Misc, etc.,
JTAG
127:0
RoadRunner Bus
127:0
127:0
26
127:0
RR Bus Interface
Slice Control Unit
DMA Subsystem
DMA Engine
Fabric Instalation
Slice Req Control
Configuration Subsystem
Dedicated Logic
28
LSM
DPU
CTL
30
Tile 0
Re-Configurable Logic
Tile 2
Slice 0
Slice 1
Slice 2
Slice 3
Programmable IO
502-009.eps

FIGURE 1

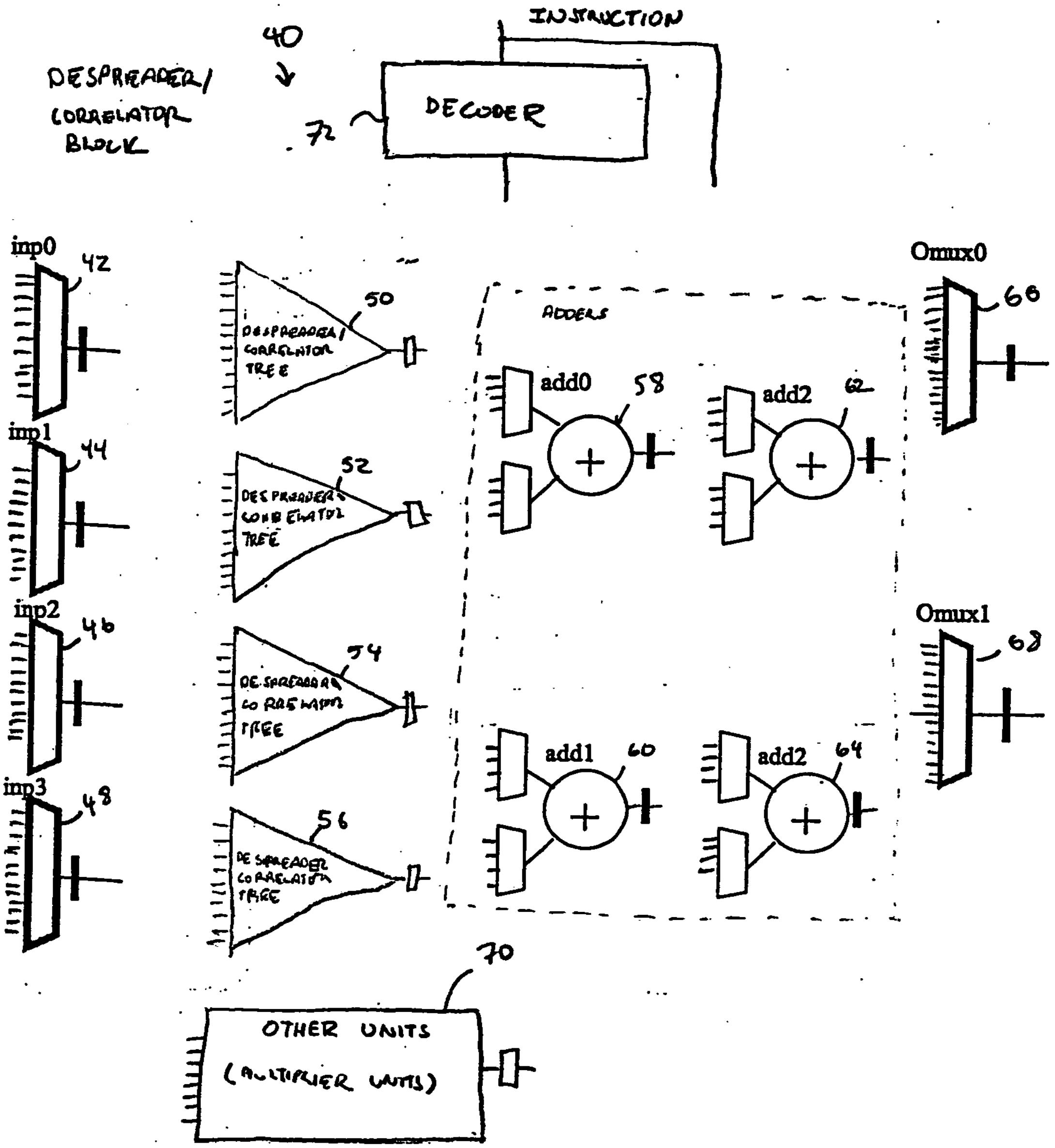

INSTRUCTION
40
DESPREADER/
CORRELATOR
BLOCK
72
DECODER
inp0
42
inp1
44
inp2
46
inp3
48
50
DESPREADER/
CORRELATOR
TREE
52
DESPREADER/
CORRELATOR
TREE
54
DESPREADER/
CORRELATOR
TREE
56
DESPREADER/
CORRELATOR
TREE
ADDERS
add0
58
add2
62
add1
60
add2
64
Omux0
66
Omux1
68
70
OTHER UNITS
(MULTIPLIER UNITS)

FIGURE 2

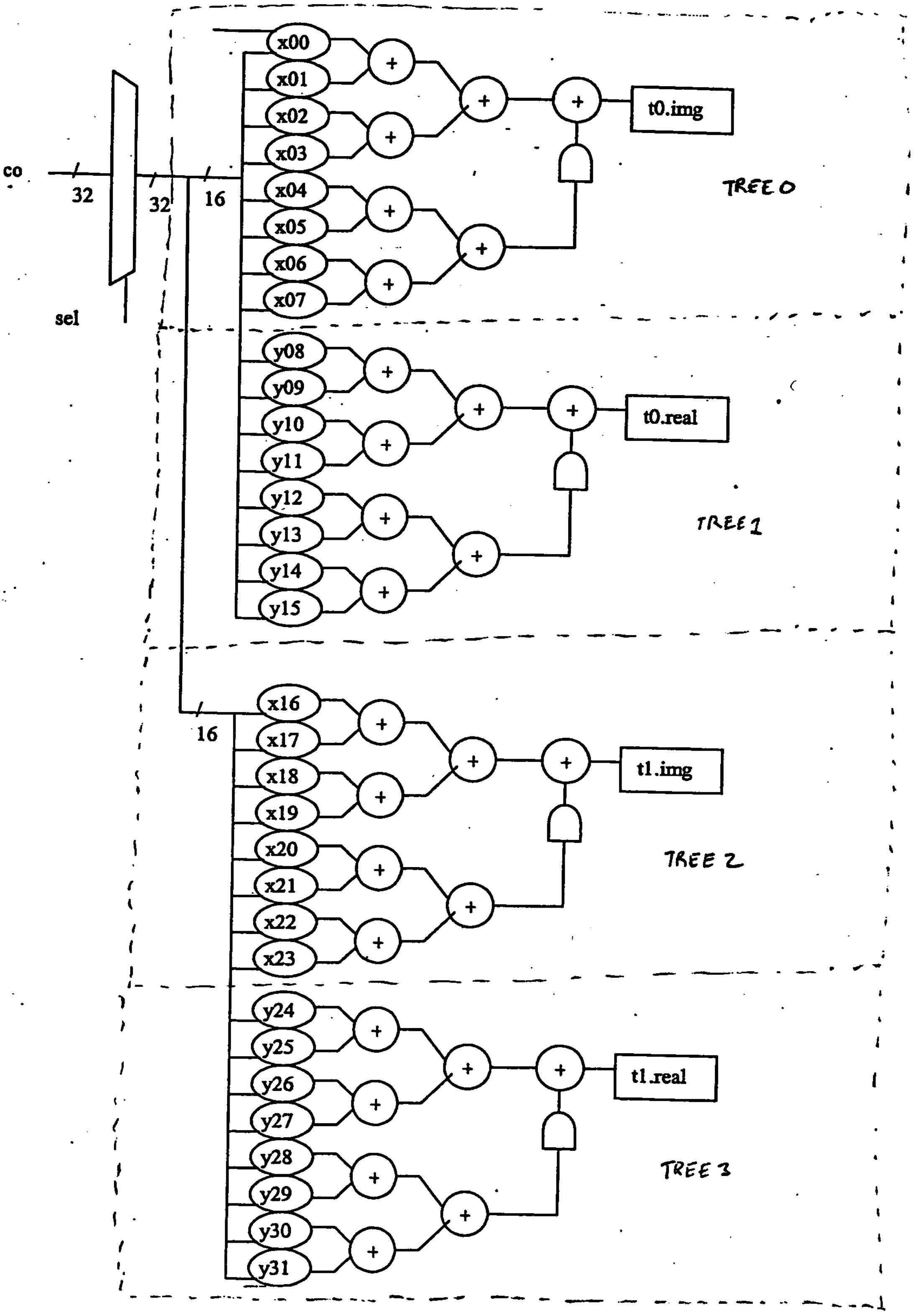

co
32
32
16
sel
x00
x01
x02
x03
x04
x05
x06
x07
t0.img
TREE 0
y08
y09
y10
y11
y12
y13
y14
y15
t0.real
TREE 1
16
x16
x17
x18
x19
x20
x21
x22
x23
t1.img
TREE 2
y24
y25
y26
y27
y28
y29
y30
y31
t1.real
TREE 3

FIGURE 3

CODE (real,img)	mapping	result.real	result.img
00	+1,+1	+r	+i
01	+1,-1	+i	-r
10	-1,+1	-i	+r
11	-1, 1	-r	-i

OPCODE	Despreader	4XDESP	8XDESP	16XCorrelate
mux negate unit		C src bit	C src bit	C src bit
x00	T0.img	c[0,1]	c[0,1]	c[0,1]
x01	T0.img	c[2,3]	c[4,5]	c[2,3]
x02	T0.img	c[4,5]	c[8,9]	c[4,5]
x03	T0.img	c[6,7]	c[12,13]	c[6,7]
x04	T0.img	-	c[2,3]	c[8,9]
x05	T0.img	-	c[6,7]	c[10,11]
x06	T0.img	-	c[10,11]	c[12,13]
x07	T0.img	-	c[14,15]	c[14,15]
y08	T0.real	c[0,1]	c[0,1]	c[0,1]
y09	T0.real	c[2,3]	c[4,5]	c[2,3]
y10	T0.real	c[4,5]	c[8,9]	c[4,5]
y11	T0.real	c[6,7]	c[12,13]	c[6,7]
y12	T0.real	-	c[2,3]	c[8,9]
y13	T0.real	-	c[6,7]	c[10,11]
y14	T0.real	-	c[10,11]	c[12,13]
y15	T0.real	-	c[14,15]	c[14,15]
x16	T1.img	c[16,17]	c[16,17]	c[16,17]
x17	T1.img	c[18,19]	c[20,21]	c[18,19]
x18	T1.img	c[20,21]	c[24,25]	c[20,21]
x19	T1.img	c[22,23]	c[28,29]	c[22,23]
x20	T1.img	-	c[18,19]	c[24,25]
x21	T1.img	-	c[22,23]	c[26,27]
x22	T1.img	-	c[26,27]	c[28,29]
x23	T1.img	-	c[30,31]	c[30,31]
y24	T1.real	c[16,17]	c[16,17]	c[16,17]
y25	T1.real	c[18,19]	c[20,21]	c[18,19]
y26	T1.real	c[20,21]	c[24,25]	c[20,21]
y27	T1.real	c[22,23]	c[28,29]	c[22,23]
y28	T1.real	-	c[18,19]	c[24,25]
y29	T1.real	-	c[22,23]	c[26,27]
y30	T1.real	-	c[26,27]	c[28,29]
y31	T1.real		c[30,31]	c[30,31]

Figure 4

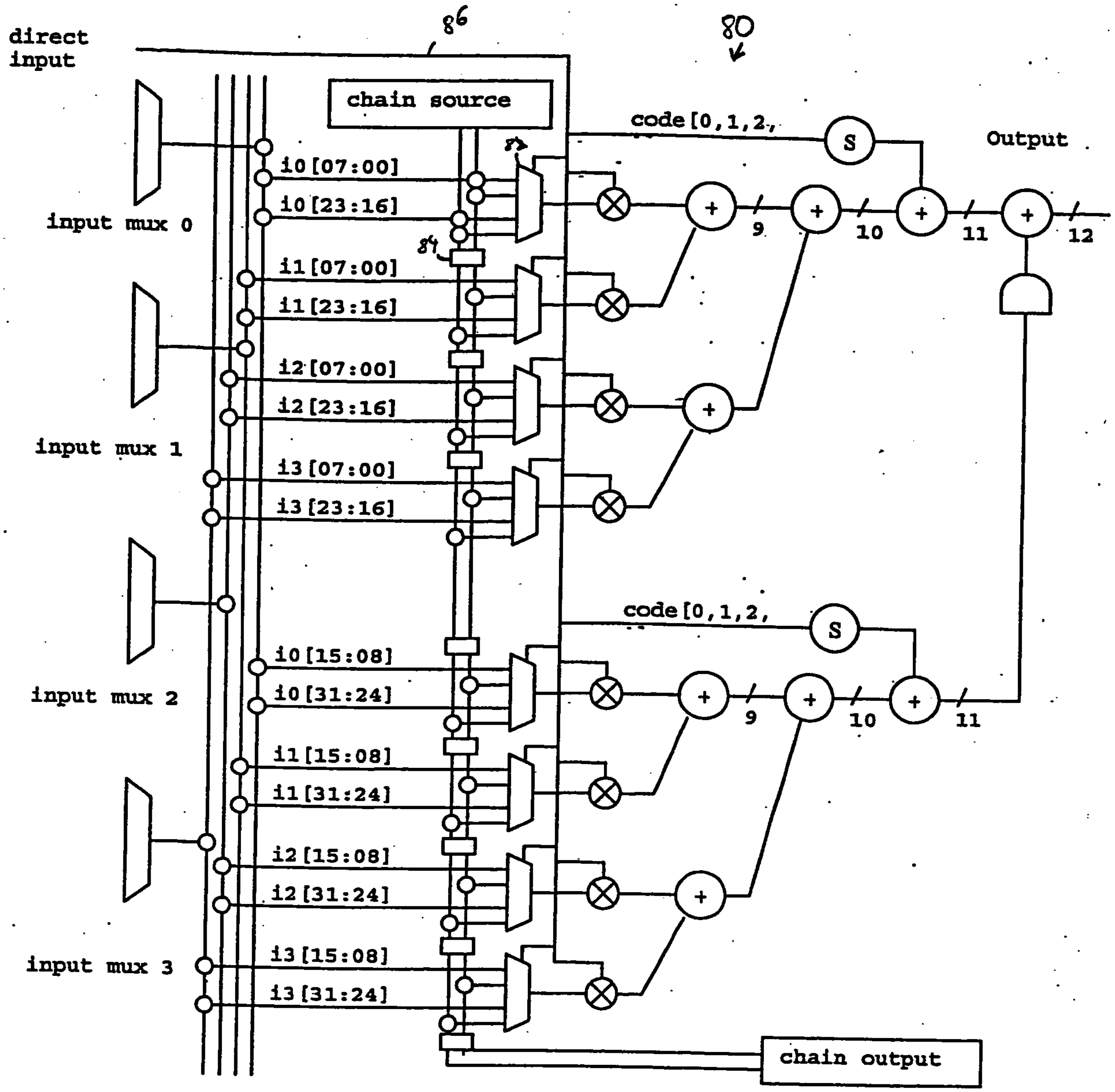

86
80
direct input
chain source
code [0,1,2,
S
Output
82
i0 [07:00]
i0 [23:16]
input mux 0
84
9
10
11
12
i1 [07:00]
i1 [23:16]
i2 [07:00]
i2 [23:16]
input mux 1
i3 [07:00]
i3 [23:16]
code [0,1,2,
S
i0 [15:08]
i0 [31:24]
input mux 2
9
10
11
i1 [15:08]
i1 [31:24]
i2 [15:08]
i2 [31:24]
input mux 3
i3 [15:08]
i3 [31:24]
chain output

FIGURE 5

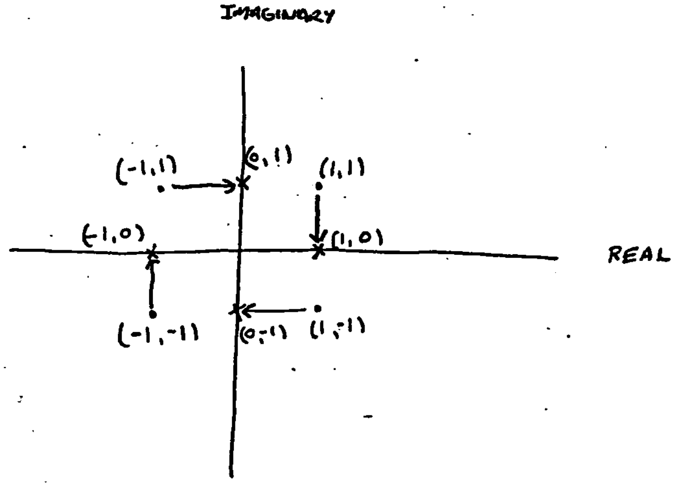


FIGURE 6B

PN CODE	MAPPING	45° rotated scaled:	COMPLEX MULTIPLICATION	RESULT
00	(1,1)	(1,0)	1 • (a + jb)	(a + jb)
01	(1,-1)	(0,-1)	-j • (a + jb)	(b - ja)
11	(-1,-1)	(-1,0)	-1 • (a + jb)	(-a - jb)
10	(-1,1)	(0,1)	j • (a + jb)	(-b + ja)

FIGURE 6A

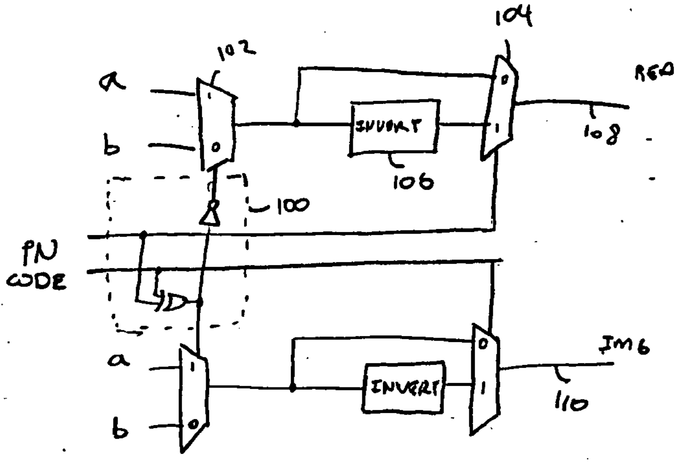


FIGURE 7A

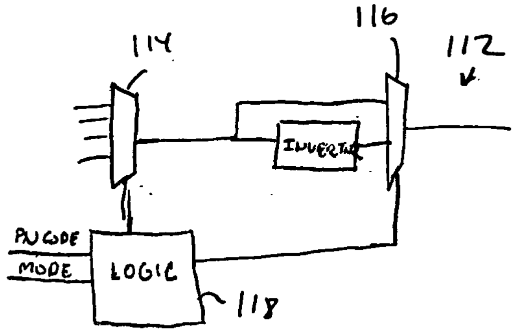
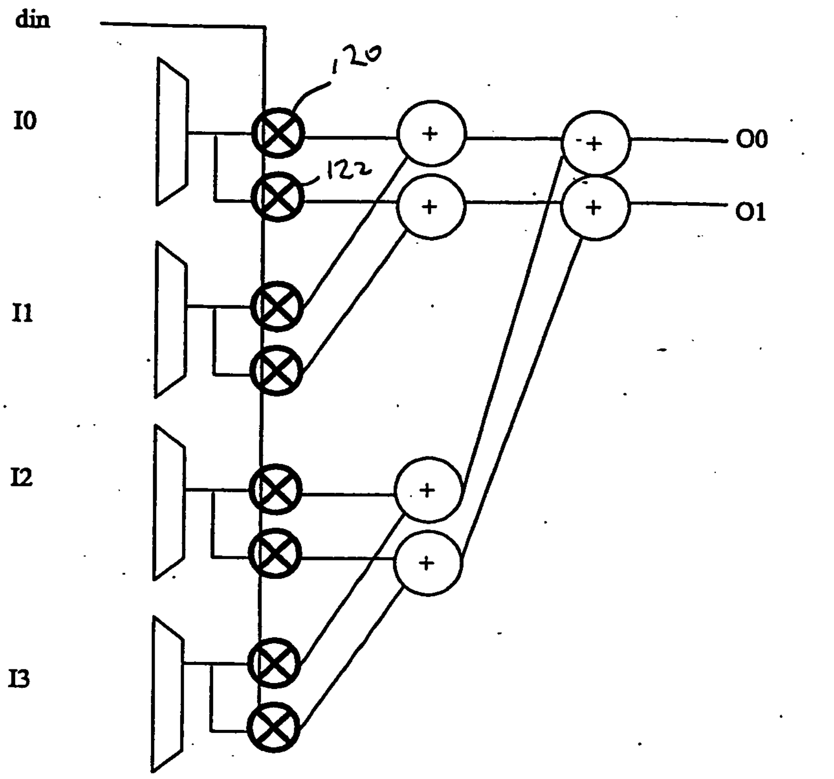
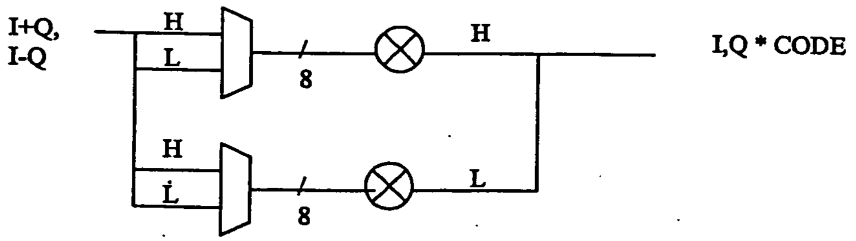


FIGURE 7B

Despreading Implementation 1

The diagram below implements a 4 chip despreader to two different CODE codes





16-bit implementation of despreading opcode

CODE	O[31:16]=	O[15:0]=
00	-H=-(I-Q)	L=-(I+Q)
01	-L=-(I+Q)	H=(I-Q)
10	L= (I+Q)	-H=-(I-Q)
11	H= (I-Q)	L=(I+Q)

CODE(real,img)	result.real	result.img
00 -> -1,-1	-(r - i)	-(r + i)
01 -> -1, 1	-(r + i)	r - i
10 -> 1,-1	r + i	-(r - i)
11 -> 1, 1	r - i	r + i

FIGURE 8

Function	Output	Function
Despreader Trees0	O0[15:00]	real - i
Despreader Trees1	O0[31:16]	imaginary - q
Despreader Trees2	O1[15:00]	real - i
Despreader Trees3	O1[31:16]	imaginary - q

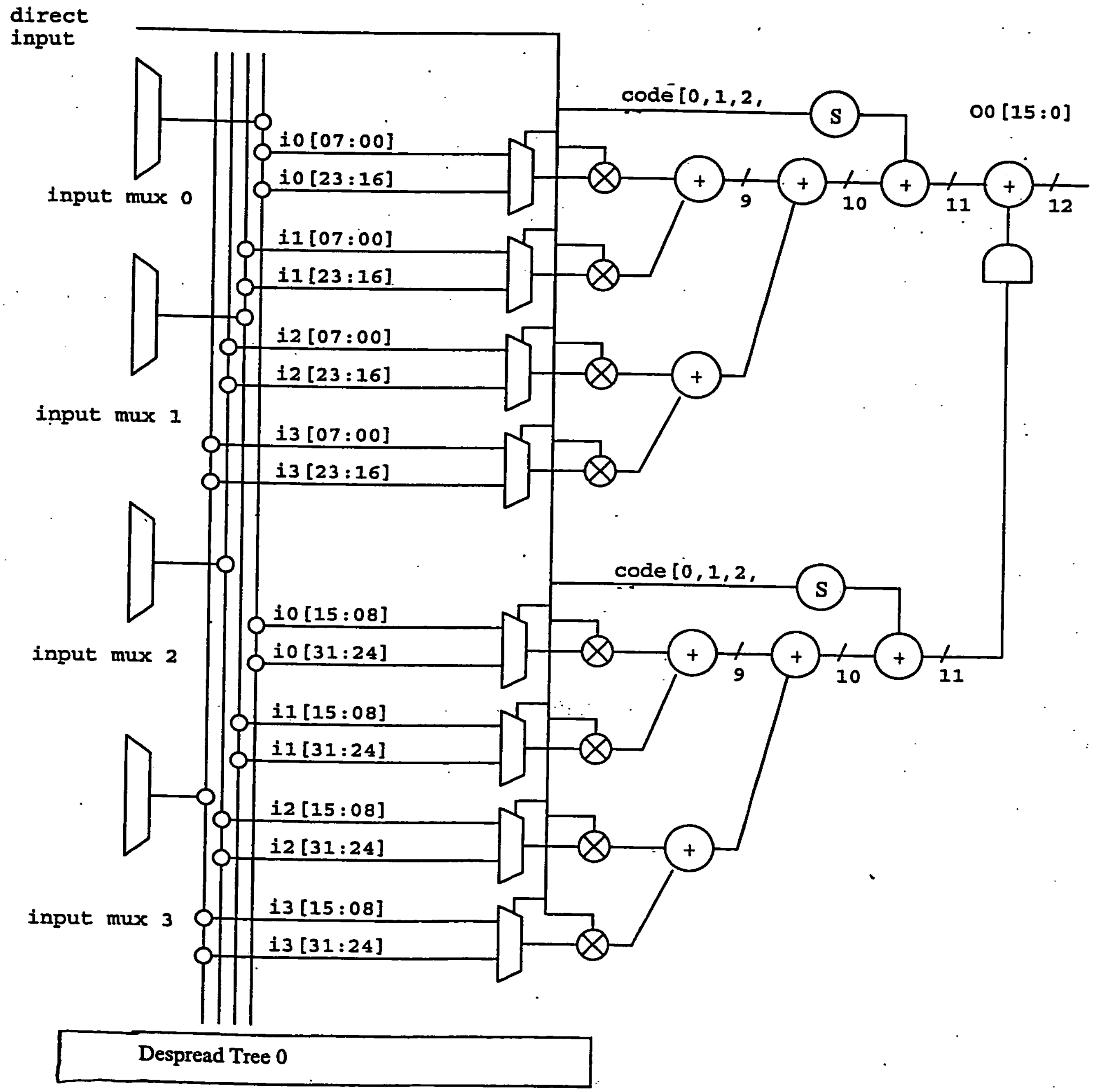


FIGURE 9

Despreader integration with input and Output muxes

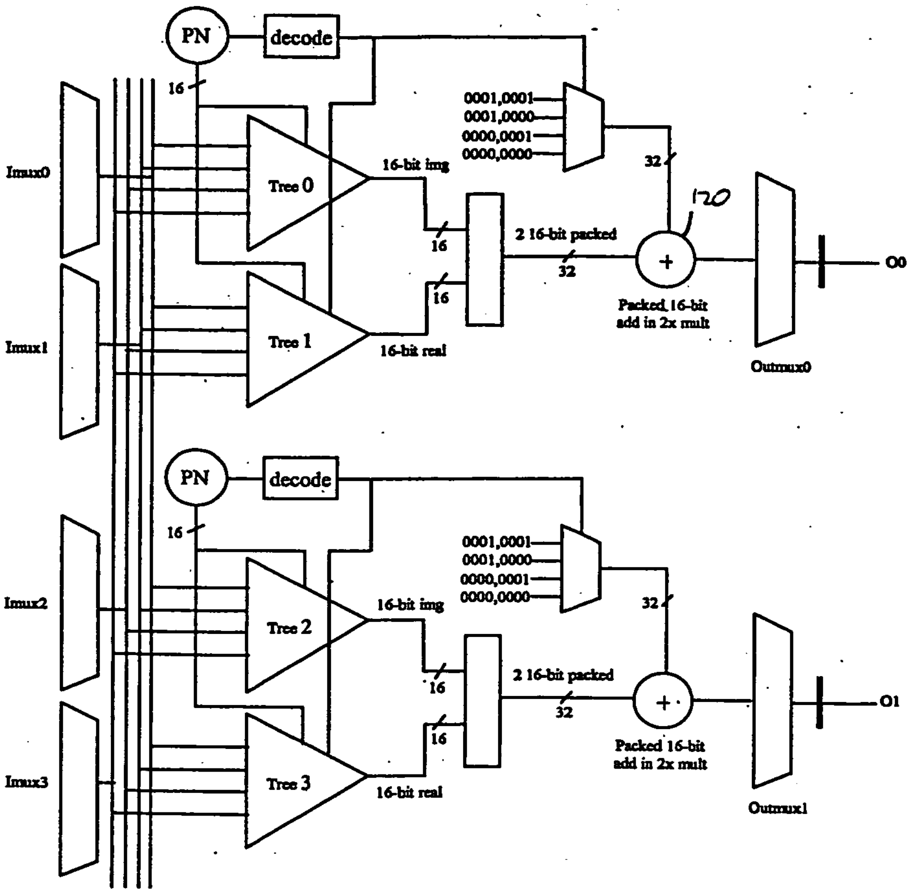


FIGURE 10

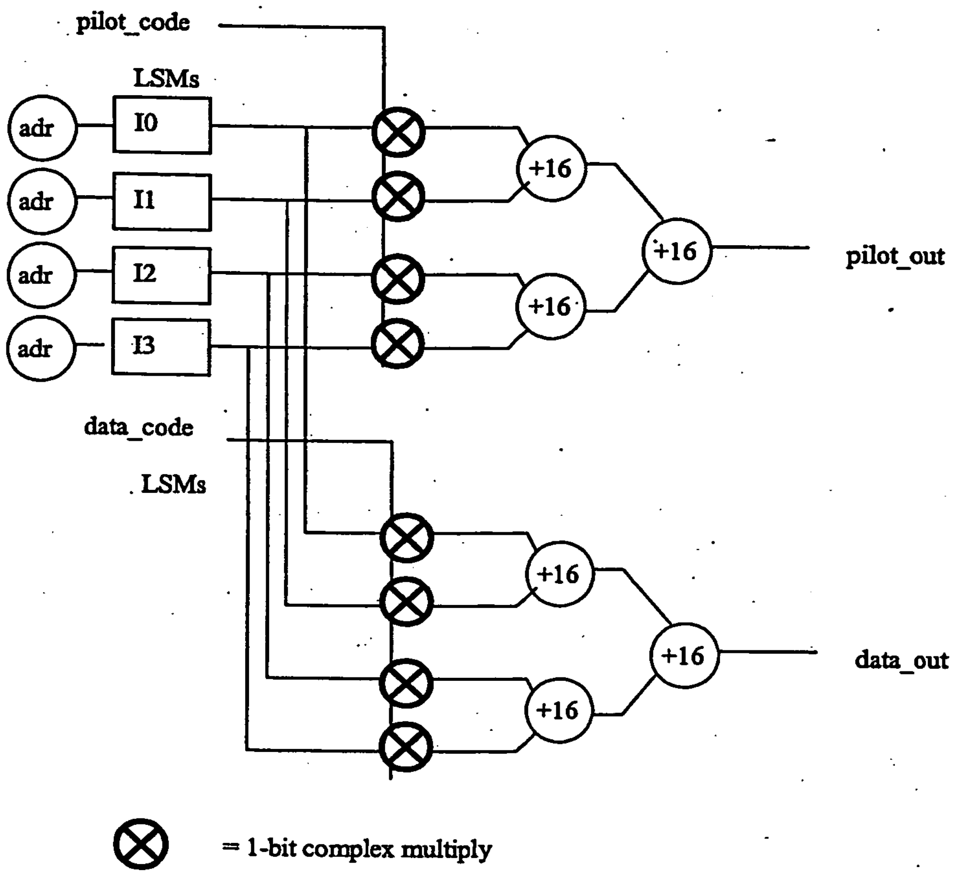

pilot_code
LSMs
adr
I0
adr
I1
adr
I2
adr
I3
+16
+16
+16
pilot_out
data_code
LSMs
+16
+16
+16
data_out
= 1-bit complex multiply

FIGURE 11

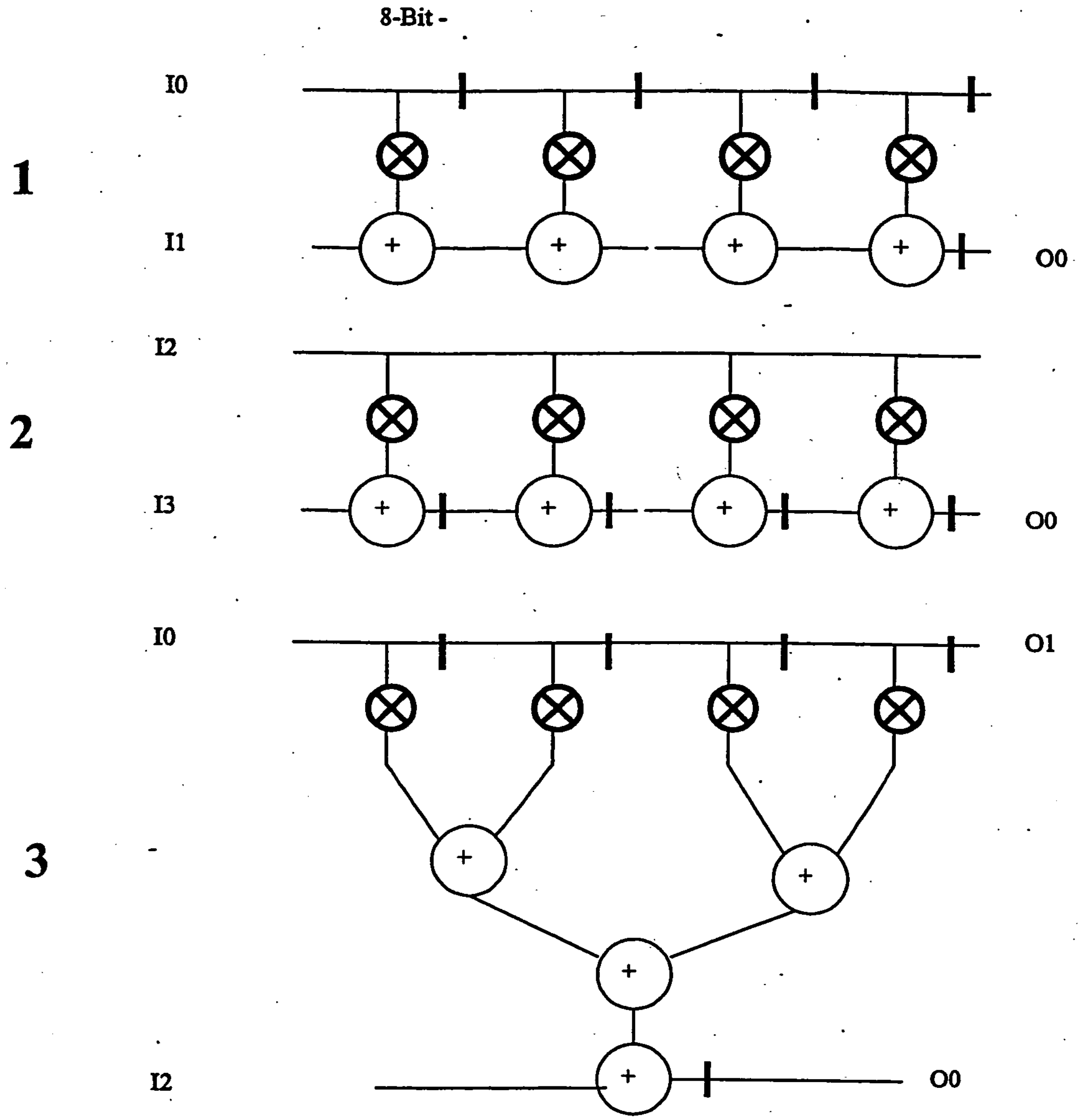
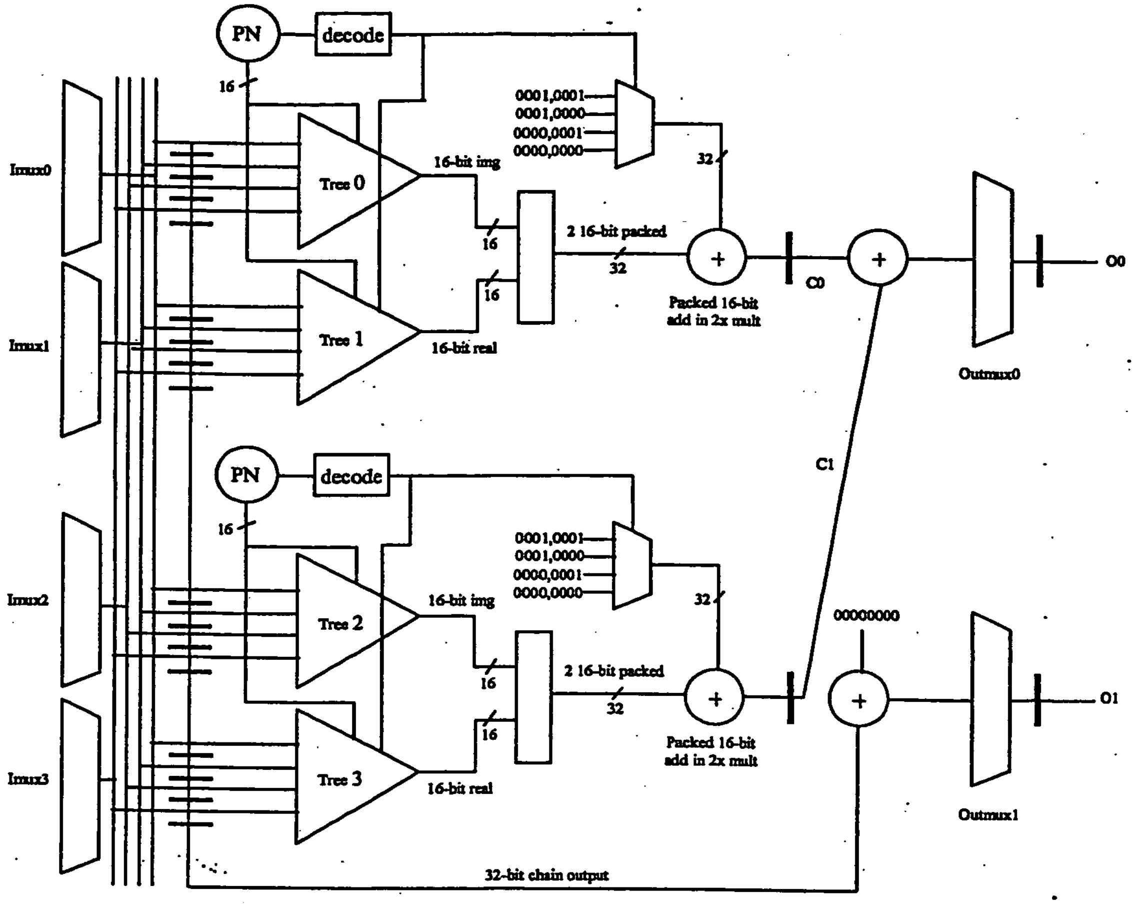


FIGURE 12



- 32-bit chain output is added with all zero in the 2x mult before being sent to output mux 1.
- 2 32-bit packed outputs C0 and C1 are added together before being sent to output mux 0.

FIGURE 13

mode	code	real result	img result
complex	00	real	img
complex	01	img	-real
complex	10	-img	real
complex	11 0	-real	-img
complex-cnj	01 0	real	img
complex-cnj	00 1	img	-real
complex-cnj	11 0	-img	real
complex-cnj	10 1	-real	-img
real-r*	0x	real	
real-r	1x	-real	
real-i**	x0		img
real-i	x1		-img
zero	xx	real	img

* real mode selects the real input and uses code[1] to control negation for the real output.
** real mode select the img input and uses code[0] to control negation for the img output.

FIGURE 14

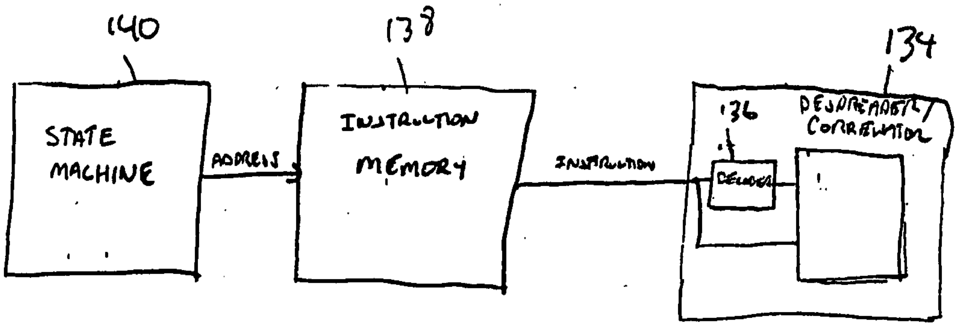


FIGURE 16.

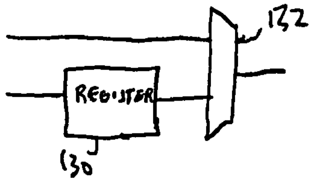


FIGURE 15.

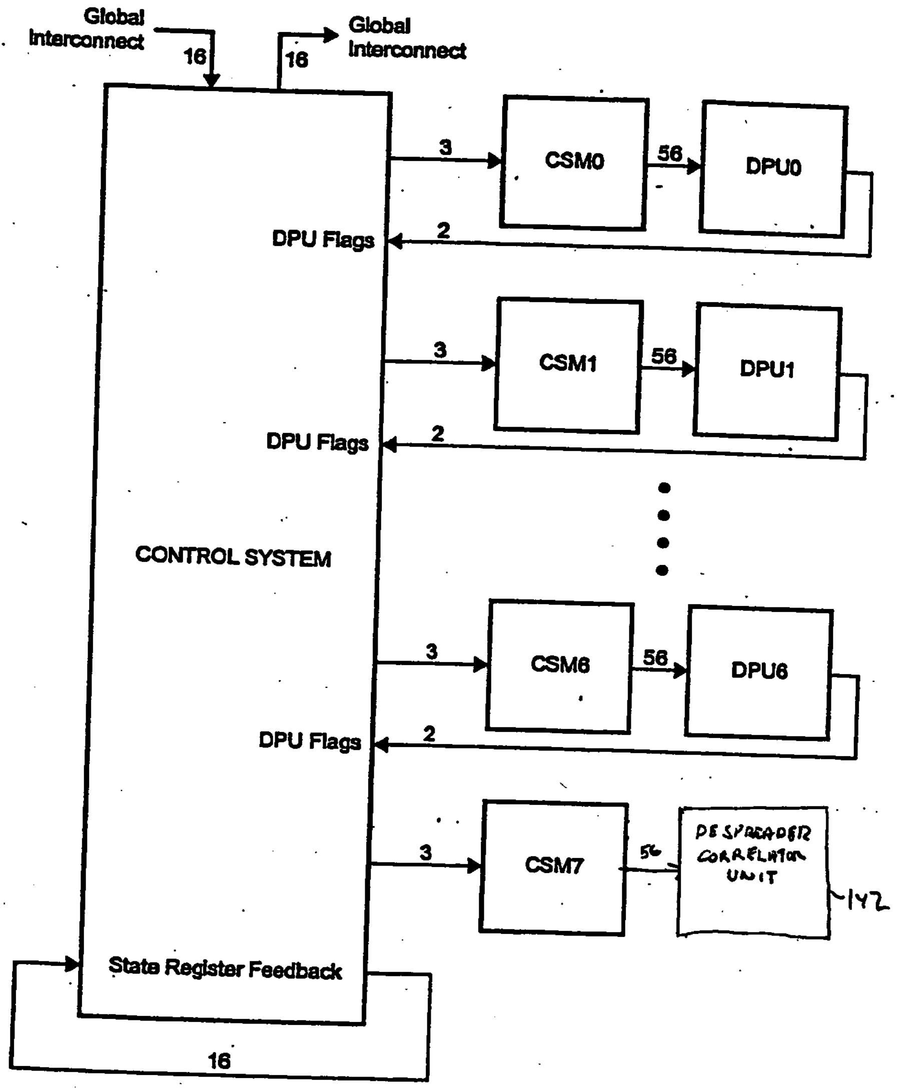

Global
Interconnect
16
16
Global
Interconnect
3
CSM0
56
DPU0
DPU Flags
2
3
CSM1
56
DPU1
DPU Flags
2
CONTROL SYSTEM
3
CSM6
56
DPU6
DPU Flags
2
3
CSM7
56
DESPREADER
CORRELATOR
UNIT
142
State Register Feedback
16

FIGURE 17

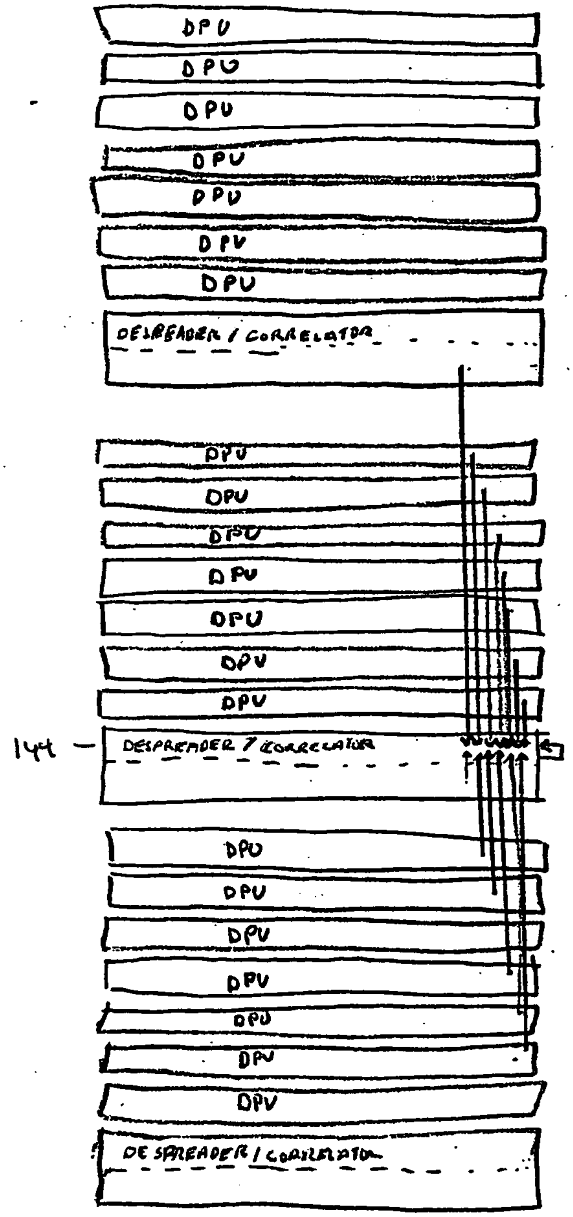

DPU
DPU
DPU
DPU
DPU
DPU
DPU
DESPREADER / CORRELATOR
DPU
DPU
DPU
DPU
DPU
DPU
DPU
144
DESPREADER / CORRELATOR
DPU
DPU
DPU
DPU
DPU
DPU
DPU
DESPREADER / CORRELATOR

FIGURE 18

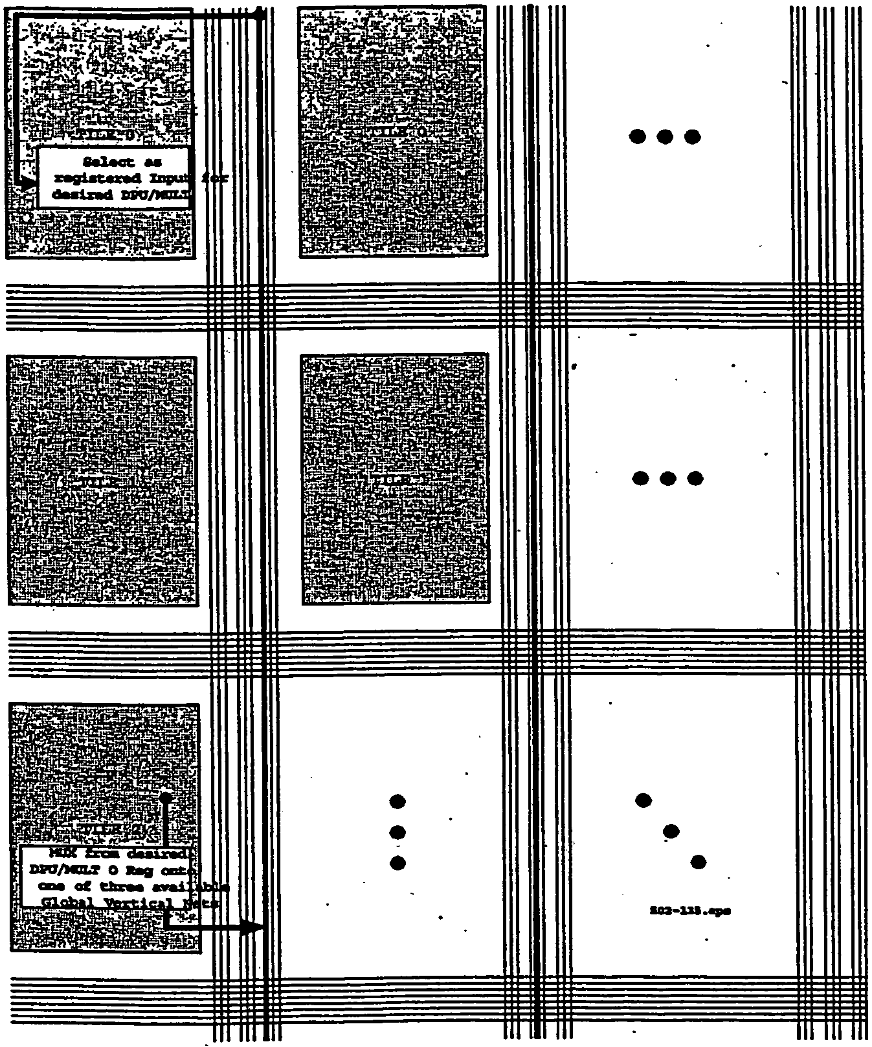

TILE 0
Select as
registered Input for
desired DPU/MULT
TILE 0
TILE 2
MUX from desired
DPU/MULT O Reg onto
one of three available
Global Vertical Nets
S02-133.eps

FIGURE 19

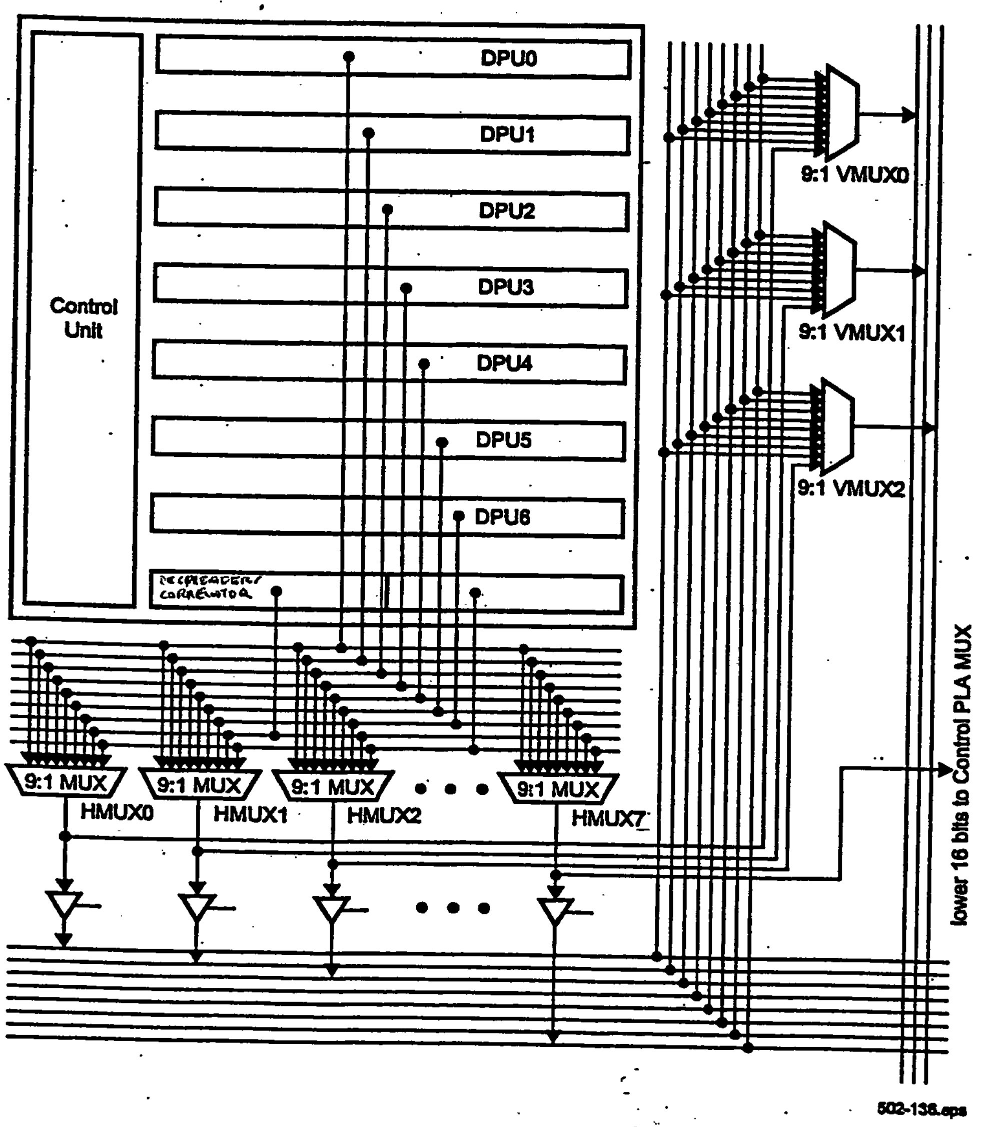

Control Unit
DPU0
DPU1
DPU2
DPU3
DPU4
DPU5
DPU6
DESPREADER/ CORRELATOR
9:1 VMUX0
9:1 VMUX1
9:1 VMUX2
9:1 MUX
HMUX0
9:1 MUX
HMUX1
9:1 MUX
HMUX2
9:1 MUX
HMUX7
lower 16 bits to Control PLA MUX
502-138.eps

FIGURE 20

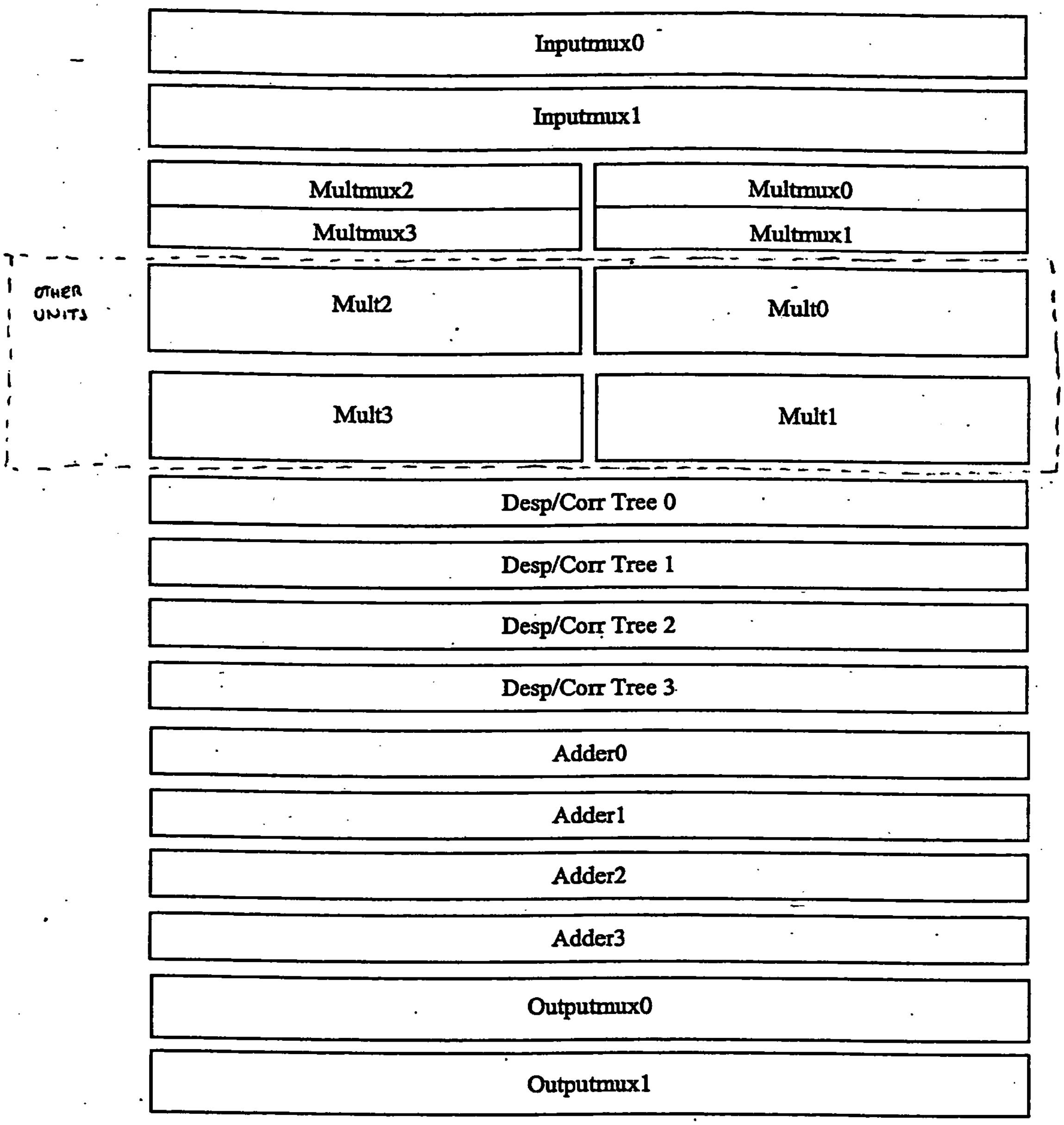

Inputmux0
Inputmux1
Multmux2
Multmux3
Multmux0
Multmux1
OTHER UNITS
Mult2
Mult0
Mult3
Mult1
Desp/Corr Tree 0
Desp/Corr Tree 1
Desp/Corr Tree 2
Desp/Corr Tree 3
Adder0
Adder1
Adder2
Adder3
Outputmux0
Outputmux1

FIGURE 21

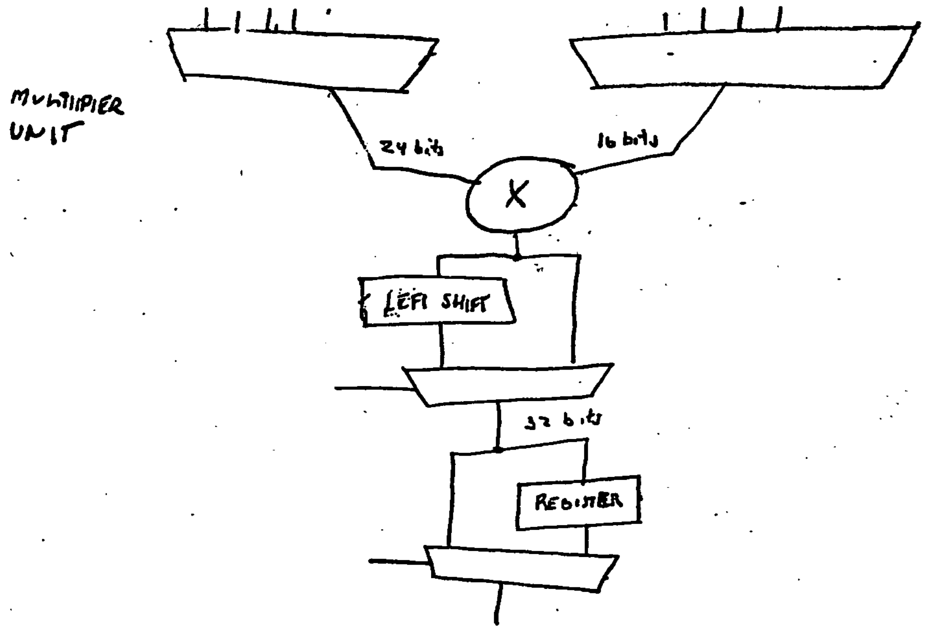


FIGURE 22A

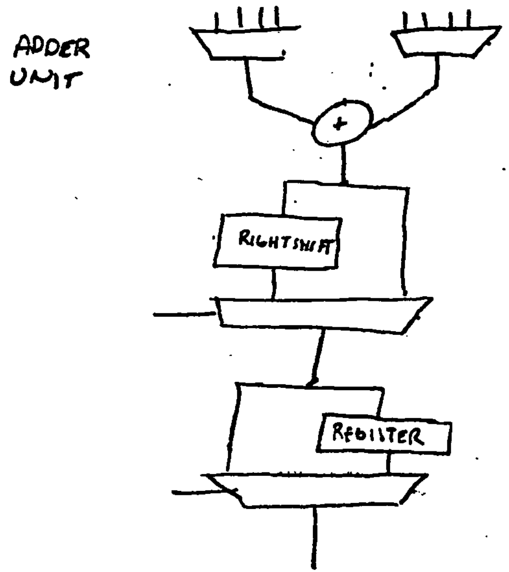


FIGURE 22B

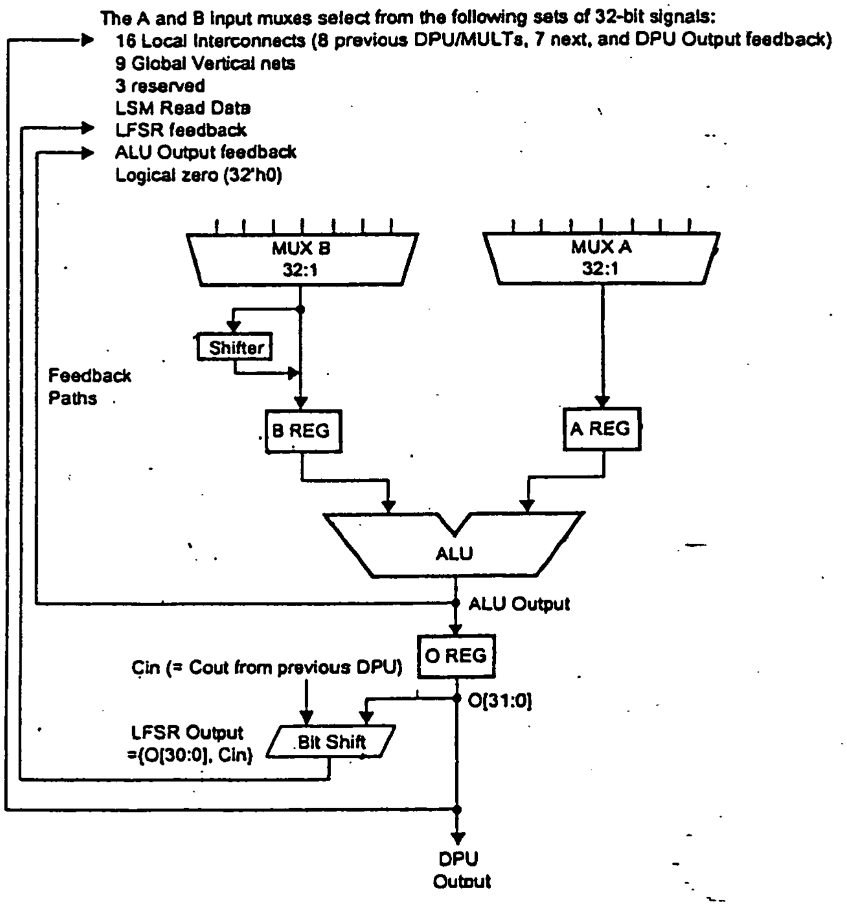

The A and B input muxes select from the following sets of 32-bit signals:
16 Local Interconnects (8 previous DPU/MULTs, 7 next, and DPU Output feedback)
9 Global Vertical nets
3 reserved
LSM Read Data
LFSR feedback
ALU Output feedback
Logical zero (32'h0)
MUX B
32:1
MUX A
32:1
Shifter
Feedback
Paths
B REG
A REG
ALU
ALU Output
O REG
Cin (= Cout from previous DPU)
O[31:0]
LFSR Output
={O[30:0], Cin}
Bit Shift
DPU
Output

FIGURE 23